UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,621	03/10/2004	Enrico Temporiti Milani	851863.411	4753

38106 7590 06/03/2005

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
LUU, AN T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,621	TEMPORITI MILANI ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 5-8 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. There is no additional limitation of a phase detector recited in dependent claim 5. In fact, claim 5 calls for a phase locked loop circuit wherein the independent claim calls for a phase detector which is commonly known as a component of the phase locked loop circuit.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by the Partovi et al reference (U.S. Patent 5,963,059).

Partovi et al discloses in figure 8 a phase detector comprising a first bistable element 804 clocked by the first signal Fin and having a first output (i.e., output of 808) a second bistable element 802 clocked by the second signal Fref and having a second output signal (i.e., output of 806); means for determining the change of said phase difference signal (i.e., charge pump as shown in fig 1), responsive to said first and second output signals, and a reset circuit 810 having

a first and a second inputs respectively connected to said first and second output signals and adapted to determine the resetting of the first and the second bistable elements responsive to the attainment of a respective prescribed state on the part of the first and the second output signals, said first and second inputs of the reset circuit substantially symmetrical to each other from the point of view of a respective input impedance associated with each of them (i.e., 832 and 830 are symmetrically coupled to 828) as required by claim 1.

As to claim 2, inverter 832 and 830 are seen as input impedance symmetrization means.

As to claim 3, fig. 8 discloses a logic circuit 828 with a first logic input and a second logic input, respectively coupled to the first and the second signals and adapted to detect the attainment of the respective prescribed state by the first and the second output signals, and in which said symmetrization means are associated with said first and second logic inputs.

As to claim 5, figure 1 discloses a phase difference detector 102 adapted to detect a phase difference between the reference signal (Fin) and a signal derived from the output signal (Fout), and an oscillator 106 controlled by a phase difference signal (output of 102) generated by the phase difference detector, characterized in that the phase difference detector is realized according to claim 1 (See the rejection of claim 1 as noted above).

As to claim 8, it is inherent that there exists a generator to generate a reference signal.

As to claim 9, it is rejected for reciting a method/step derived from an apparatus of claim 1 which is rejected as noted above.

As to claim 10, the scope of claim is similar to that of claim 1. Therefore, it is rejected for the same reason set forth above.

4. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by the Nilsson reference (U.S. Patent 6,605,935).

Nilsson disclose in fig 11 a phase detector comprising a first bistable element 1001 clocked by the first signal (fref) and having a first output (source) a second bistable element 1003 clocked by the second signal (Presc) and having a second output signal (sink); means for determining the change of said phase difference signal (charge pump; 1105 and 1107), responsive to said first and second output signals, and a reset circuit 1109 having a first and a second inputs respectively connected to said first and second output signals and adapted to determine the resetting of the first and the second bistable elements responsive to the attainment of a respective prescribed state on the part of the first and the second output signals, said first and second inputs of the reset circuit substantially symmetrical to each other from the point of view of a respective input impedance associated with each of them (i.e., 1113 and 1115 are symmetrically coupled to 1109) as required by claim 1.

As to claim 2, delays 1113 and 1115 are seen as input impedance symmetrization means.

As to claim 3, fig. 11 discloses a logic circuit 1109 with a first logic input and a second logic input, respectively coupled to the first and the second signals and adapted to detect the attainment of the respective prescribed state by the first and the second output signals, and in which said symmetrization means are associated with said first and second logic inputs.

As to claim 4, the symmetrization means 1113 and 1115 are seen as decoupling means of the first and second inputs (i.e., being enable) of the reset circuit from the first and second logic inputs, respectively.

As to claim 5, figure 2 discloses a phase difference detector 201 adapted to detect a phase difference between a reference signal (i.e., output of RERF. OSCF) and a signal derived from the output signal (Fout), and an oscillator 209 controlled by a phase difference signal (output of 201) generated by the phase difference detector, characterized in that the phase difference detector is realized according to claim 1 (See the rejection of claim 1 as noted above).

As to claims 6 and 7, figure 2 and its associated description disclose the frequency divider 205 being an N-fractional divider controlled by delta-sigma modulator 211. Therefore, its dividing factor is either an integer number or an average division factor equal to a non-integer number.

As to claim 8, it is inherent that there exists a generator to generate a reference signal.

As to claim 9, it is rejected for reciting a method/step derived from an apparatus of claim 1 which is rejected as noted above.

As to claim 10, Nilsson discloses in figure 11 a phase detector 1100 comprising a first logic element 1101 having an input terminal coupled to receive a first clock signal (fref), and having an output terminal (source), a second logic element 1103 having an input terminal coupled to receive a second clock signal (Presc) and having an output terminal (sink); a feedback circuit (block comprising 1111, 1109,1113 and 1115) having two inputs and an output, a first input being coupled to the output terminal of the first logic element and a second input coupled to the output of the second logic circuit (See fig. 11), a feedback line (i.e., line coupling feedback circuit and RESET terminals) coupled from the output of the feedback circuit to a control input terminal in each of the first and second logic elements, and a phase correction circuit (i.e., charge pump 1105 and 1107) coupled to the output of the first logic element and to the output of the

second logic element and providing at its output (Iout) a phase correction signal as required by the claim.

As to claim 11, fig.11 shows a delay circuit 1111 for providing a timed delay from the outputs to the control inputs of the first and second logic elements.

As to claim 12, fig.11 shows the control input terminal being a feedback terminal.

As to claim 13, the feedback circuit further includes a logic gate 1109 coupled to the first and second outputs from the first and second logic elements and outputs a signal to the delay circuit 1111.

As to claim 14, delays 1113 and 1115 are seen as a symmetrization element coupled to the first and second outputs of the first and second logic elements.

Allowable Subject Matter

5. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the limitation "*the symmetrization element includes two transistors having control terminals coupled to the respective first and second output terminals of the first and second logic elements*" as required by claim 15.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
5-26-05

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800